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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/523,717

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Masakazu Sagawa

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EXAMINER

PERRY, ANTHONY T

ART UNIT

PAPER NUMBER

2879

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

# Office Action Summary

**Application No.**

10/523,717

**Applicant(s)**

SAGAWA ET AL.

**Examiner**

ANTHONY T. PERRY

**Art Unit**

2879

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 July 2008.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SF/ICE)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Specification***

The amendment filed 7/03/08 is objected to under 35 U.S.C. 132(a) because it introduces new matter into the disclosure. 35 U.S.C. 132(a) states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: there is no support that the second interlayer insulation layer is a "non-anodic" insulation film. There is support in the spec that the second insulation layer is formed by a "deposition process", however, this does not necessarily mean that the layer cannot be an anodic insulation layer.

Applicant is required to cancel the new matter in the reply to this Office Action.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is lack of support in the specification, as originally filed, for the second insulation film being a non-anodic insulation film.

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 5-7, 10, 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kusunoki et al. (US 5,936,257).

Regarding claim 1, Kusunoki et al. disclose a cold cathode type flat panel display comprising: a first substrate (14) including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode (13), an upper electrode (11) and an electron acceleration layer (12) retained between said lower electrode and said upper electrode (11), each of said thin-film type electron sources emitting electrons from said upper electrode (11) in response to a voltage applied between said lower electrode (13) and said upper electrode (11); and a second substrate (not shown) including a fluorescent screen in which a plurality of phosphors to be excited by said electrons emitted from said first substrate are arrayed; said cold cathode type flat panel display being characterized in that each of said arrays of said thin-film type electron sources includes an anodic oxide insulation layer (12) and an upper electrode feeder wiring (32) serving as a power feed line to said upper electrode (11); and a non-anodic oxide insulation layer (15) is provided between said anodic oxide layer (12) and said upper electrode feeder wiring (32) (for example, see Fig. 3A and col. 8, lines 19-39).

Regarding claim 2, Kusunoki et al. teach that the lower electrode (13) is made of aluminum or an aluminum alloy; said electron acceleration layer (portion of item 12 located

between the upper electrode (11) and lower electrode (13)) and said anodic oxide layer (portion of item 12 located below insulating layer (15)) are anodic oxide films of said aluminum or aluminum alloy forming said lower electrode; and said non-anodic insulation layer (15) is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films of said aluminum or aluminum alloy forming said lower electrode (13) (for example, see col. 19-39).

Regarding claim 3, Kusunoki discloses a terminal portion of said non-anodic insulation film (15) surrounding an electron acceleration region (12) has a normal dip shape (for example, see Fig. 3A).

Regarding claim 5, Kusunoki discloses a cold cathode type flat panel display comprising: a first substrate (14) including thin-film type electron sources arranged in arrays, each of said thin-film type electron sources including a lower electrode (13), an upper electrode (11) and an electron acceleration layer (12) retained between said lower electrode and said upper electrode (11), each of said thin-film type electron sources emitting electrons from said upper electrode (11) in response to a voltage applied between said lower electrode (13) and said upper electrode (11); and a second substrate (not shown) including a fluorescent screen in which a plurality of phosphors to be excited by said electrons emitted from said first substrate are arrayed; said cold cathode type flat panel display being characterized in that each of said arrays of said thin-film type electron sources includes an anodic oxide insulation layer (12) and an upper electrode feeder wiring (32) serving as a power feed line to said upper electrode (11); and a non-anodic oxide insulation layer (15) having an opening and provided between said anodic oxide layer (12) and said upper electrode feeder wiring (32); and wherein a region for emitting electrons is

defined by a region of said opening of said non-anodic insulation layer (15) (for example, see Fig. 3A and col. 8, lines 19-39).

Regarding claim 6, Kusunoki teaches that the lower electrode (13) is made of aluminum or an aluminum alloy; said electron acceleration layer (12) and said anodic oxide layer are anodic oxide films of said aluminum or aluminum alloy forming said lower electrode; and said non-anodic insulation layer (15) is made of an insulation film material which can be etched selectively with respect to said lower electrode and said anodic oxide films of said aluminum or aluminum alloy forming said lower electrode (13) (for example, see col. 19-39).

Regarding claim 7, Kusunoki discloses a terminal portion of said non-anodic insulation layer (15) surrounding an electron acceleration region (12) has a normal dip shape (for example, see Fig. 1).

Regarding claims 10 and 13, Kusunoki teaches the non-anodic insulation layer being formed of an oxide (for example, see col. 8, lines 36-39).

Regarding claims 12 and 15, Kusunoki teaches the non-anodic insulation film having the same structural form and made of the same material as the Applicant's insulation film, and therefor teaches the functional language, "said non-anodic insulation film enables covering of defects unevenly distributed in a boundary between an electron acceleration layer and said anodic oxide film and enables suppression of a time-dependent insulation breakdown." It is elementary that mere recitation of a newly discovered function or property, inherently possessed by things in the prior art, does not cause a claim drawn to distinguish over the prior art.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 4, 8-9, 11, and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kusunoki et al. (US 5,936,257).

Regarding claims 4 and 8-9, Kusunoki discloses non-anodic insulation film (15) has a normal dip shape in a terminal portion thereof surrounding an electron emission region, said normal dip shape being formed using a difference in etching rate among said layers (for example, see Fig. 6 and paragraphs 0014-0015).

Kusunoki does not specifically recite that the non-anodic film has a structure of a plurality of layers. However, it is noted that the applicant's specific limitation of the non-anodic insulation film containing a plurality of layers, does not solve any of the stated problems or yield any unexpected result that is not within the scope of the teachings applied. Therefore it is considered to be a matter of choice, which a person of ordinary skill in the art would have found obvious to select any number of layers of insulation material for the non-anodic insulation film, as long as the non-anodic film includes a normal dip shape at terminal portions thereof, defining the tunneling area.

The Examiner notes that the claim limitation that "said normal dip shape being formed using a difference in etching rate among said layers" is drawn to a process of manufacturing which is incidental to the claimed apparatus. It is well established that a claimed apparatus cannot be distinguished over the prior art by a process limitation. Consequently, absent a

showing of an unobvious difference between the claimed product and the prior art, the subject product-by-process claim limitation is not afforded patentable weight (see MPEP 2113). Therefore, it is the position of the examiner that it would have been obvious to one of ordinary skill in the art that the dip shape disclosed by JP 7-65710 is at least a fully functional equivalent to the Applicant's claimed dip shape as evidenced by JP 7-65710 suggestion of all of the Applicant's claimed structural limitations.

Regarding claims 11 and 14, Kusunoki et al. do not specifically recited that the non-anodic film is a nitride film. However, it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. Silicon nitride layers and silicon oxide layers used as insulation layers are known to be interchangeable when used as passivation layers. Thus, it would have been obvious to one having ordinary skills in the art at the time the invention was made to have used any type of insulation layer an oxide, nitride, or a combination thereof, since the selection of known materials for a known purpose is within the skill of the art.

#### **Contact Information**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Anthony Perry* whose telephone number is (571) 272-2459. The examiner can normally be reached between the hours of 9:00AM to 5:30PM Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nimesh Patel, can be reached on (571) 272-2457. **The fax phone number for this Group is (571) 273-8300.**



Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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